LZ95G71

Single-chip Driver LSI for CCD

DESCRIPTION

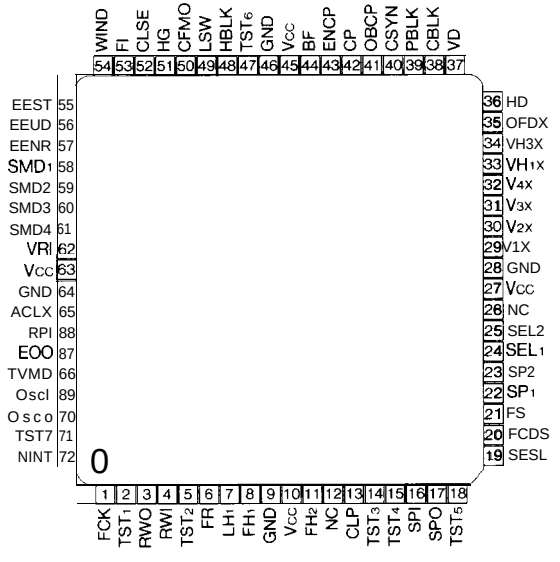
The LZ95G71 is a CMOS single chip driver LSI which provides timing pulses used to drive a CCD area sensor, and generates synchronous pulses for TV signals and processing pulses for video signals.

FEATURES

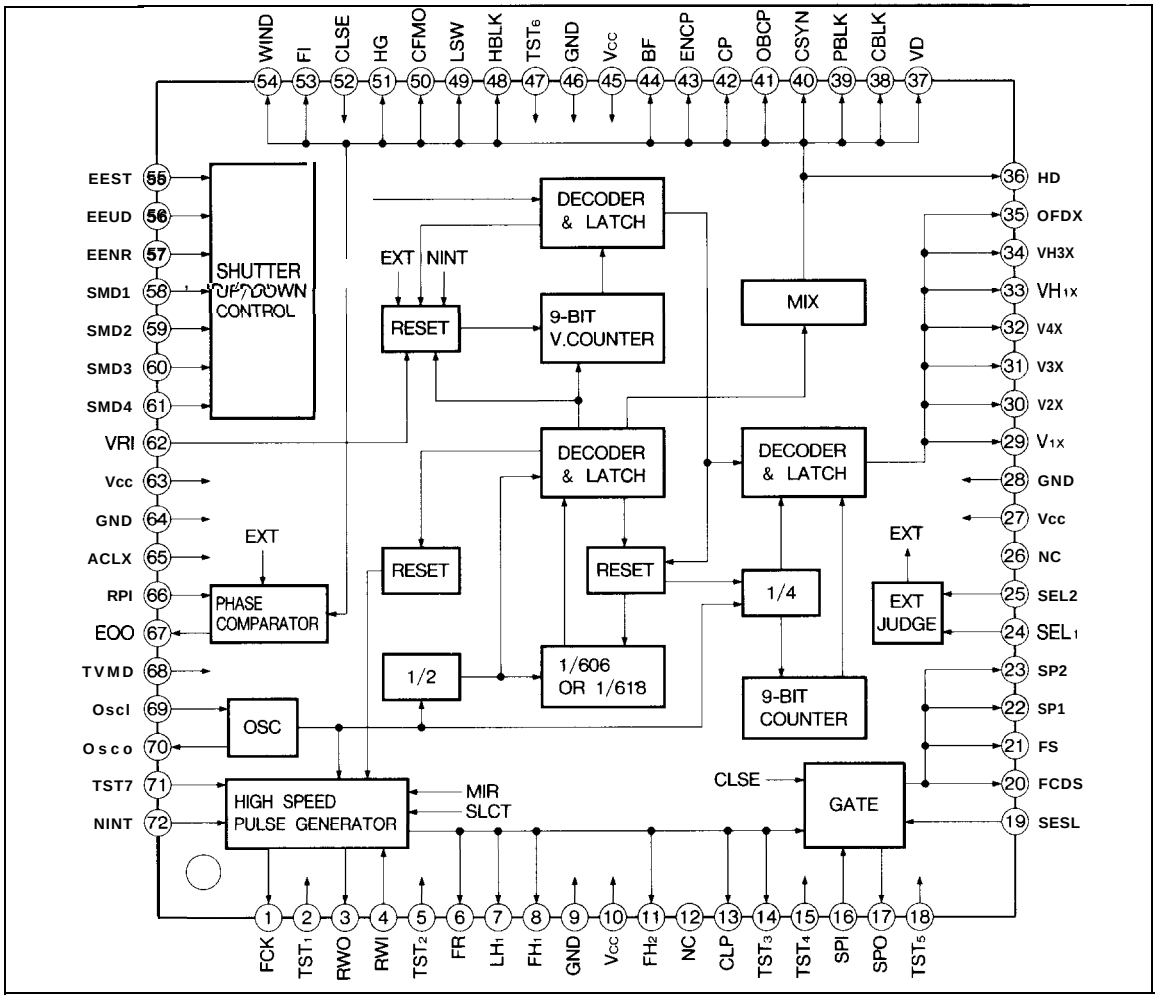
- Switchable **between 410000 pixels CCD and 470000 pixels CCD**
- Switchable **between NTSC (EIA) and PAL (CCIR) systems**
- **Built-in EE (Electronic Exposure) control (1/60 to 1/100000 s for NTSC; 1/50 to 1/100 000 s for PAL)**
- **Internal electronic shutter :**
  Shutter speed is selectable from 1/60 (PAL :1 /50), 1 /250, 1 /500, 1/1 000, 1/2 000, 1/4 000 and 1/1 00000 s, in addition to this, 1/1 00 (PAL : 1/120 s) in Flicker-less mode using parallel code
- Swichable **between Electronic Shutter mode and EE Control mode**
- **Single + 5 V power supply**
- **Package : 72-pin QFP(QFP072-P-101 O)**

PIN CONNECTIONS

72-PIN QFP **TOP VIEW**



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	− 0.3 to 7.0	v
Input voltage	VI	−0.3 to V_{CC} + 0.3	v
Output voltage	Vo	−0.3 to V_{CC} + 0.3	v
Operating temperature	Topr	−20 to +70	℃
Storage temperature	Tstg	−55 to +150	℃

DC CHARACTERISTICS

(V_{CC} = +5 V ± 10%, Ta=−20 to +70℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Low voltage	V_{IL}				1.5	v	1
Input High voltage	V_{IH}		3.5			v	
Input Low voltage	V_{T+}				3.7	v	2
Input High voltage	V_{T-}		1.0			v	
Hysteresis voltage	$V_{T+} - V_{T-}$		0.4			v	
Input Low current	$\lvert I_{IL1} \rvert$	Vl=0 v			1,0	μA	3
	$\lvert I_{IL2} \rvert$	Vl=0 v	8.0		70	μA	4
Input High current	$\lvert I_{IH1} \rvert$	VI= Vcc			1.0	μA	5
	$\lvert I_{IH2} \rvert$	V_I = Vcc	8,0		70	μA	6
Output High voltage	V_{OH} 1	I_{OH} = −2 mA	4.0			v	7
Output Low voltage	V_{OL1}	I_{OL} = 4 mA			0.4	v	
Output High voltage	V_{OH2}	I_{OH} = − 3 mA	4.0			v	8
Output Low voltage	V_{OL2}	I_{OL} = 4 mA			0,4	v	
Output High voltage	V_{OH3}	I_{OH} = −6 mA	4.0			v	9
Output Low voltage	V_{OL3}	I_{OL} = 8 mA			0.4	v	
Output High voltage	V_{OH4}	I_{OH} = −9 mA	4.0			v	10
Output Low voltage	V_{OL4}	I_{OL} = 12 mA			0.4	v	
Output High voltage	V_{OH5}	I_{OH} = −9 mA	4.0			v	11
Output Low voltage	V_{OL5}	I_{OL} = 18 mA			0,4	v	
Output High voltage	V_{OH6}	I_{OH} = −6 mA	4.0			v	12
Output Low voltage	V_{OL6}	I_{OL} = 12 mA			0.4	v	
Leak output current	$\lvert I_{OZ} \rvert$	**High-Z**			1.0	μA	

NOTES :

1. Applied to inputs (IC, ICD, ICU).
2. **Applied to input** (ICSU).
3. **Applied to inputs** (IC, ICD).
4. **Applied to inputs** (ICU, ICSU).
5. **Applied to inputs** (IC, ICU, ICSU).
6. **Applied to input (ICD).**
7. **Applied to outputs (O, OR1 ,** OSC)
   (Output (OSC) **measures on conditions that input** (IBF0) **level is O V or** V_{CC}).
6. **Applied to output (ORA).**
9. **Applied to output (ORB).**
10. **Applied to output** (ORC).
11. **Applied to output** (ORD).
12. **Applied to** tri-state **output (TO).**

PIN FUNCTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	FCK	o		Clock output for delay line	A pulse for clock of CCD delay line. The frequency of the signal is 1/2 frequency of the OSCI.
2	TSTI	ICD	–	Test terminal 1	A test pin. Sat open or to L level in the Normal mode.
3	RWO	o		Width of FR control output	A pulse to control pulse width of FR (pin 6). Connect to RWI (pin 4) pin through CR delay circuit.
4	RWI	IC	–	Width of FR control input	An input pin to control pulse width of FR. Falling edge of FR is defined by leading edge of input pulse.
5	TST2	ICD	–	Test terminal 2	A test pin. Sat open or to L level in the Normal mode.
6	FR	o		Reset pulse	A reset pulse for CCD. Connect to ϕ_R of CCD through the DC offset circuit.
7	LH_1	o		Horizontal transfer last pulse	A pulse to drive the last gate of horizontal CCD. Connect to LH_1 of CCD.
8	FH_1	o		Horizontal transfer pulse 1	A horizontal transfer pulse for CCD. Connect to ϕH_1 of CCD
9	GND	–	–	Ground	A grounding pin.
10	V_{CC}	–	–	Power supply	Supply +5 V power.
11	FH2	o		Horizontal transfer pulse 2	A horizontal transfer pulse for CCD. Connect to ϕH_2 of CCD
12	NC	–	–	No-connection	A pin for no use,
13	CLP	o		Clamp pulse	A pulse to clamp dummy output of CCD. The repetition is horizontal frequency.
14	TST3	ICD	–	Test terminal 3	A test pin. Sat open or to L level in the Normal mode,
15	TST4	ICD	–	Test terminal 4	
16	SPI	IC	–	Phase of SPI, SP2 control input	An input pin to control pulse phase of SPI, SP2.
17	SPO	o		Phase of SP_1, SP2 control output	A pulse to control pulse phase of SP_1, SP2. Connect to SPI (pin 16) pin through the CR delay circuit.
18	TST5	ICD	–	Test terminal 5	A test pin. Sat open or to L level in the Normal mode.
19	SESL	ICU	–	SPO control input	An input pin to switch phase of SPO. H level or open : The pulse is delayed by about 35 ns from RWO. L level : The pulse is nearly RWO pulse,

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
20	FCDS	O	⎍	CDS pulse 1	A pulse to clamp the feed-through level from CCD.
21	FS	O	⎍	CDS pulse 2	A pulse to sample-hold the signal from CCD.
22	SP1	O	⎍	Color sampling pulse 1	A pulse to output the sampling for color separation based upon the output signal of CCD.
23	SP_2	O	⎍	Color sampling pulse 2	A pulse to output the sampling for color separation based upon the output signal of CCD.
24	SELI	ICD	–	External Synchronization mode select 1	Select External Synchronization mode.
25	SEL2	ICD	–	External Synchronization mode select 2	
26	NC	–	–	No-connection	A pin for no use.
27	Vcc	–	–	Power supply	Supply + 5V power.
28	GND	–	–	Ground	A grounding pin.
29	V_{1X}	O	⎍	Vertical transfer pulse 1	A vertical transfer pulse for CCD. Connect to the 1 AX pin of vertical driver LSI.
30	V_{2X}	O	⎍	Vertical transfer pulse 2	A vertical transfer pulse for CCD. Connect to the 2AX pin of vertical driver LSI.
31	V3X	O	⎍	Vertical transfer pulse 3	A vertical transfer pulse for CCD. Connect to the 3AX pin of vertical driver LSI.
32	V4X	O	⎍	Vertical transfer pulse 4	A vertical transfer pulse for CCD. Connect to the 4AX pin of vertical driver LSI.
33	V_{HIX}	O	⎍	Read out pulse	A pulse that transfers the charge of the photodiode to the vertical shift register. Connect to the 1 BX pir of the vertical driver LSI.

SELI	SEL2	Mode description
L	L	Internal Synchronization mode
H	L	External Synchronization mode 1 : VD (negative polarity) or AC power line RPI input : leternal VD or AC power line
L	H	External Synchronization mode 2 : Composite Synchronization mode VRI input : VSYNC (negative polarity) RPI input : CSYNC (negative polarity)
H	H	External Synchronization mode 3 : HD and VD synchronization VRI input : external VD (negative polarity) RPI input : external HD (negative polarity)

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
34	VH3X	o	⎍	Read out pulse	A pulse that transfers the charge of the photodiode to the vertical shift register. Connect to the 3BX pin of the vertical driver LSI,
35	OFDX	O	u	OFD pulse output	A pulse that sweeps the charge of the photodiode for electrical shutter. Connect to OFD of CCD thrcugh the invert, level shift and DC offset circuit. It is held at H level in Normal mode.
36	HD	O	⎍	Horizontal drive pulse	The pulse occurs at the start of lines.
37	VD	O	⎍	Vertical drive pulse	The pulse occurs at the start of every field.
38	CBLK	O	⎍	Composite blanking pulse	Composite blanking pulse,
39	PBLK	O	⎍	Pre-blanking pulse	Equivalent to CBLK (pin 8) pulse except for shorter pulse width with cut-off falling edge.
40	CSYN	o	⎍	Composite synchronizing pulse	Composite synchronous signal output pin.
41	OBCP	O	⎍	Optical black clamp pulse	A pulse to clamp the optical black signal. This pulse stays Low during the absence of effective pixels within the vertical blanking. The repetition is horizontal frequency.
42	CP	o	⎍	Clamp pulse	CP is the same as OBCP (pin 41) except that CP is delayed by 600 ns from OBCP.
43	ENCP	o	⎍	Encoder DC clamp pulse	A clamp pulse that is used for recovering DC level. The repetition is horizontal frequency.
44	BF	o	⎍	Burst flag	A pulse to define burst period.
45	Vcc	–	·	Power supply	Supply +5 V power.
46	GND	–	–	Ground	A grounding pin.
47	TST6	ICD	–	Test terminal 6	A test pin. Set open or to L level in the Normal mode.
48	HBLK	o	u	Horizontal blanking pulse	A pulse that corresponds to the cease period of the horizontal transfer pulse.
49	LSW	o	⎍	Line switch	The signal switches between H and L at every line in PAL mode. It is set at Low level at the 1st line of the 1st field.
50	CFMO	O	n	tiler frame output	A pulse to control color frame. Occurs at every 4 fields in NTSC mode, occurs at every 8 fields in PAL mode.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
51	HG	o	⎍	Line index pulse	The pulse is used in color separtor. The signal switches between H end L at every line. For details, see "NOTES 1".
52	CLSE	ICD	–	Color sampling pulse control input	An input pin to control SP 1, SP2 pulse correspond to color separator in signal processor. CLSE input: Output to sample hold at color separator. L level or open: SPI : Output contain Ye signal. SP2 : Output contain Cy signal. HG pulse: SP1 : Output contain Mg signal. SP2 : Output contain G signal.
53	FI	o	⎍	Field index	The pulse is used for detecting field. At NTSC mode : ODD field; Low EVEN field; High At PAL mode : 1st and 3rd fields; Low 2nd and 4th fiekds; High
54	WIND	o	u	Wind pulse	A pulse for wind pulse, When conected to EEST (Pin 55), the operation of Electronic Exposure can be stopped at the upper side of monitor.
55	EEST	ICU	–	Electronic Exposure control 1	An input pin to control Electronic Exposure, with using EEUD (pin 56) and EENR (pin 57). L level : Electronic Exposure is stopped. H level or open : Electronic Exposure is operated.
56	EEUD	IC	–	Electronic Exposure control 2	An input pin to control Electronic Exposure, with using EENR (pin 57).
57	EENR	IC	–	Electronic Exposure control 3	An input pin to control Electronic Exposure, with using EEUD (pin 56). For details, see "NOTE 3".
58	SMDI	ICU	–	Shutter control 1	Input pins to set up fixed shutter speed or to control Electronic Exposure mode. For details, see "NOTE 2"
59	SMD2	ICU	–	Shutter control 2	
60	SMD3	ICU	–	Shutter control 3	
61	SMD4	ICU	–	Shutter control 4	
62	VRI	ICU	–	Vertical reset input	An input pin for resetting internal Vertical counter. For inputs of SELI (pin 24) and SEL2 (pin 25), input pulse and the point of resetting is changed.

SEL1	SEL2	VRI input
X	L	–
L	H	External VSYNC (negative)
H	H	External VD (negative)

X=H or L

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
63	Vcc			Power supply	Supply +5 V power
64	GND			Ground	A grounding pin
65	ACLX	ICU	–	All clear input	An input pin for resetting all internal circuit at power on,
66	RPI	ICU	–	Horizontal comparison input	An input pin for the reference signal to the phase comparator, at external synchronization mode. For inputs SELI (pin 24) and SEL2 (pin 25), input pulse is changed. SEL1 / SEL2 / RPI input L / L / – H / L / External VD (neaative) or line L / H / External CSYNC (negative) H / H / External HD (negative)
67	EOO	TO	–	Phase comparator output	At external synchronization mode, phase comparator output for input signal RPI (pin 66) and internal comparison signal. When RPI is advanced, output is High level, When RPI is delayed, output is Low level, When phases are equal, the terminal impedance is High,
68	TVMD	ICU	–	TV mode select	An input pin to select TV standards. L level : NTSC, EIA mode H level or open : PAL, CCIR mode
69	OSCI	IBFC	–	Clock input	An input pin for reference clock oscillation. The frequencies are as follws : At NTSC mode : 28,63636 MHz (1820 fH) At PAL mode : 28.37500 MHZ (1816 fH) (fH = Horizontal frequency)
70	Osco	Osc	–	Clock output	An output pin for reference clock oscillation. The output is the inverse OSCI (pin 69).
71	TST7	ICD	–	Test terminal 7	A test pin. Sat open or to L level in the Normal mode.
72	NINT	ICD	–	Non-interlace select	An input pin to select Non-interlace mode. L level or open : Interlace mode H level : Non-interlace mode

IC : Input pin (CMOS level).
ICU : Input pin (CMOS level with pull-up resistor)
Icsu : Input pin (CMOS schmitt-trigger level with pull-up resistor).
ICD : Input pin (CMOS level with pull-down resistor),
O, OR1 , ORA
ORB, ORC, ORD : Output pin.
TO Output pin (tri-state output).
IBFO lutput pin for oscillation.
Osc : Output pin for oscillation.

NOTES :

1. **Timing of HG (Line index** pulse)

TVMD (68Pin)	L (NTSC)	H (PAL)
Reset Line	271 H	318 H
Reset level	L	L

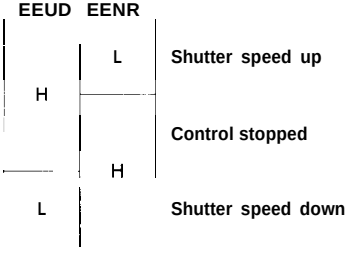
2. Fixed Shutter mode

SMD1 **(Pin 58)= Low level**

SMD2 (Pin 59)	SMD3 (Pin 60)	SMD4 (Pin 61)	SHUTTER SPEED (S)	
			NTSC	PAL
L	L	L	About 1/W	About 1 /50
H	L	L	About 1/1 00	About 1/1 20
L	H	L	About 1 /250	
H	H	L	About 1 /500	
L	L	H	About 1/1 000	
H	L	H	About 1/2 000	
L	H	H	About 1/5 000	
H	H	H	About 1/1 2000	

3. EE Control mode

SMD1 **(Pin 58) = High level**



. When EENR and EEUD are H level, control is stopped.
● When either EENR or EEUD is L level, control is resumed.
● When EEST aat to L level, EE control is disable.

SMD2 (Pin 59)	SMD3 (Pin 60)	SMD4 (Pin 61)	Shutter speed (e)
H	x	x	Maximum shutter speed : 1/1 00 000
L	x	x	Maximum shutter speed : 1/39 000
x	H	x	Start shutter speed : 1/100 000
X	L	x	Start shutter speed : 1/2 000

X=H or L

Shutter speed changes at Electronic Exposure Control mode.

NTSC			PAL		
NO.	CHARGE TIME	SHUTTER SPEED (S)	NO.	CHARGE TIME	SHUTTER SPEED (S)
1	252 H+ α	1 /62	1	302 H+ β	1 /52
	(by 10 H step)			(by 10 H step)	
19	72 H+ α	1 /218	24	72 H+ β	1/216
•	(bv 4 H step)		•	(bv 4 H step)	
30	28 H+ α	1 /557	35	28 H+ β	1 /552
•	(by 2 H step)		•	(by 2 H step)	
37	14 H+ α	1/1 102	42	14 H+ β	1/1 095
•	(bv 1 H step)		•	(by 1 H step)	
43	7 H+ α	1/2163	48	7 H+ β	1/2146
•	(by 0.5 H step)		•	(by 0.5 H step)	
50	4 H+ α	1/3 88	55	4 H+ β	1/3 655
	(by 0.25 H step)			(by 0.25 H step)	
62	1 H+ α	1/12344	67	1 H+ β	1/1 2252
	(by 0.125 H step)			(by 0.125 H step)	
70	0.280 H	1 /57 274	75	0.275 H	1 /56 750
71	0.155 H	1/105281	76	0.152 H	1/104320

α = 0.275 H β = 0.275 H

4. VRI input timing

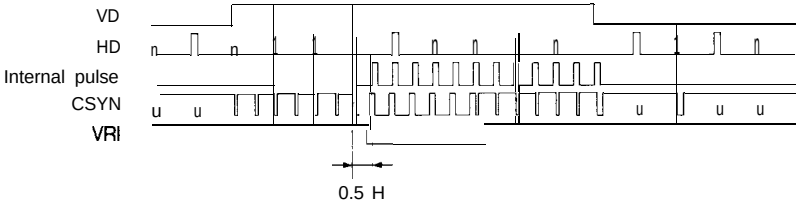
(1) Internal Synchronization mode (SEL1 = SEL2 = L)
This mode is not used for external synchronization. But if it is connected to negative polarity pulse at VRI pin, this mode is the same as External Synchronization 2.

(2) External Synchronization mode 1 (SEL1 = H, SEL2 = L)
VRI pin can't be used.

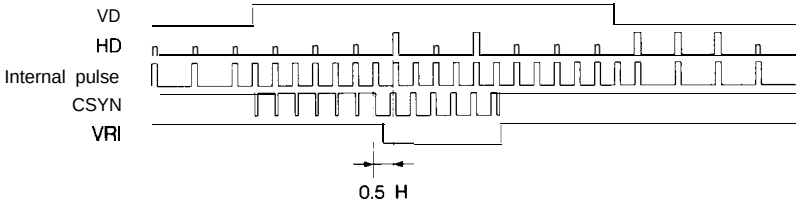
(3) External Synchronization mode 2 (SEL1 = L, SEL2 = H)
When this mode is selected, the reset-pulse (equal to VSYNC pulse : polarity is negative) which is used for internal vertical counter continu OUSI y input VRI pin from other systems.

※ About pulse timing at synchronization, please see under the figure.
(In the figure, the symbol "Internal pulse" show 2 times horizontal frequency.)

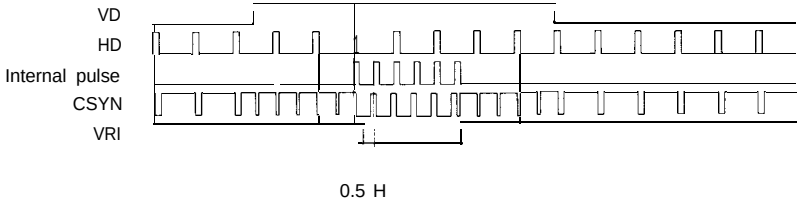
NTSC : (ODD FIELD)



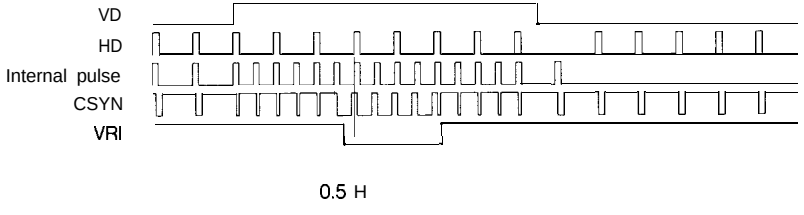
(EVEN FIELD)



PAL : (1st, 3rd FIELD)



(2nd, 4th FIELD)

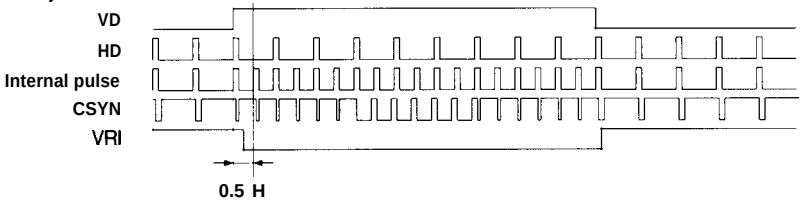


(4) External Synchronization mode 3 (SEL 1 = H, SEL2 = H)

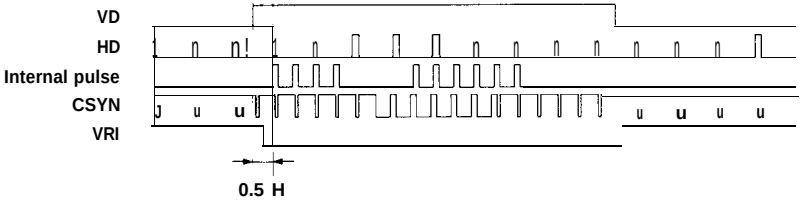
When this mode is selected, the reset-pulse (equal to VD pulse : polarity is negative) which is used for internal vertical counter continuously input VRI pin from other systems.

※ About pulse timing at synchronization, please see under the figure. (In the figure, the symbol "Internal pulse"' show 2 times horizontal frequency.)

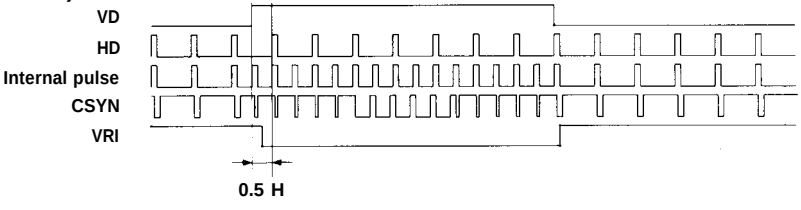
NTSC : (ODD FIELD)



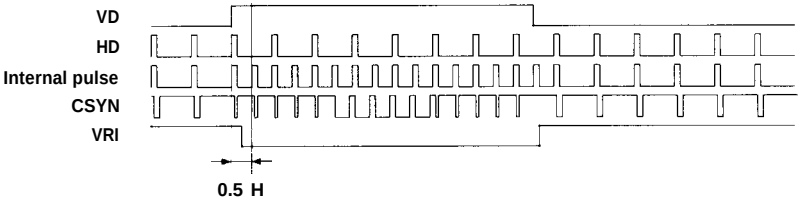
(EVEN FIELD)



PAL : (1st, 3rd FIELD)

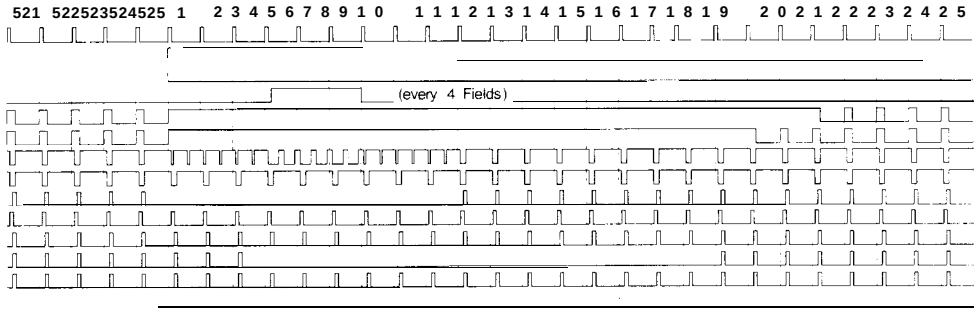


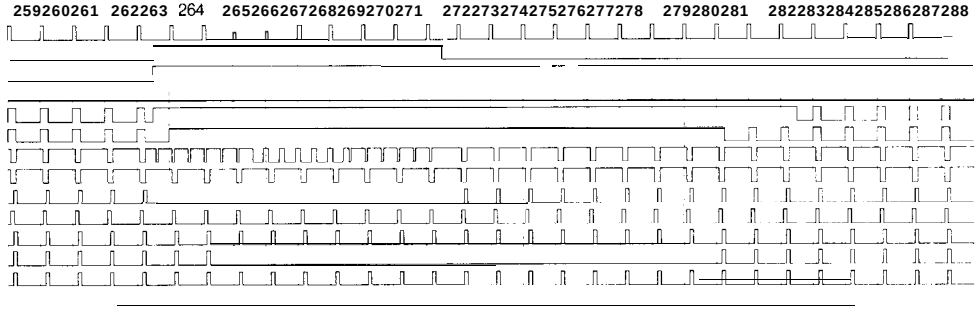
(2nd, 4th FIELD)



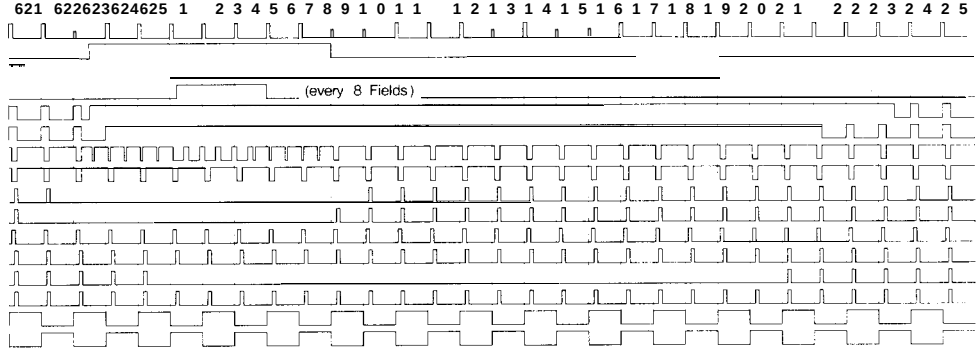
TIMING DIAGRAM

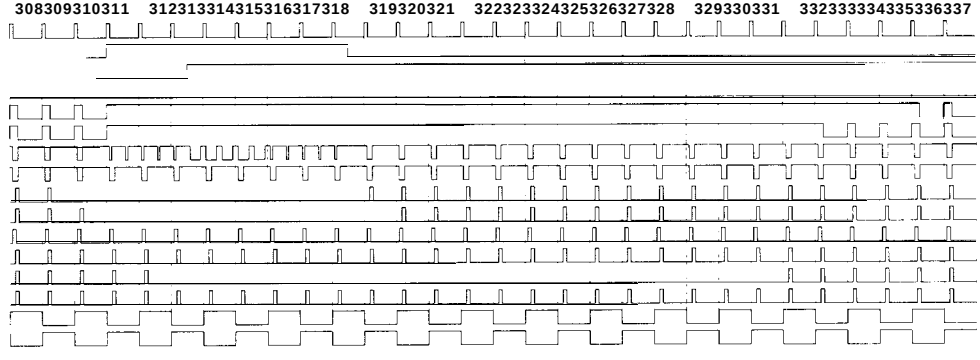
SYNCHRONIZING VERTICAL PULSE < NTSC >





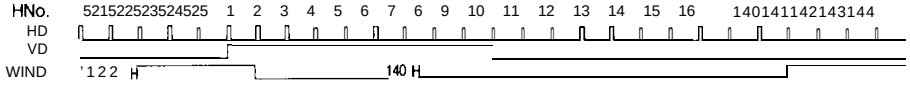
SYNCHRONIZING VERTICAL PULSE < PAL >



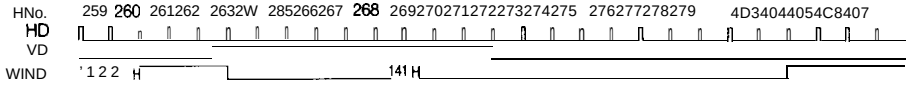


SYNCHRONIZING VERTICAL PULSE

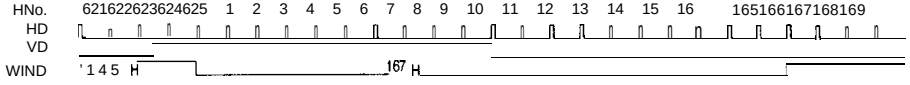
NTSC : (ODD FIELD)



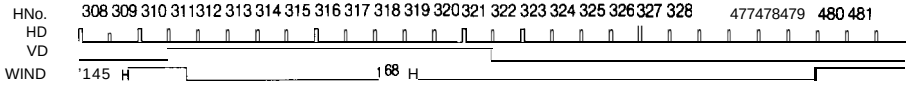
(EVEN FIELD)



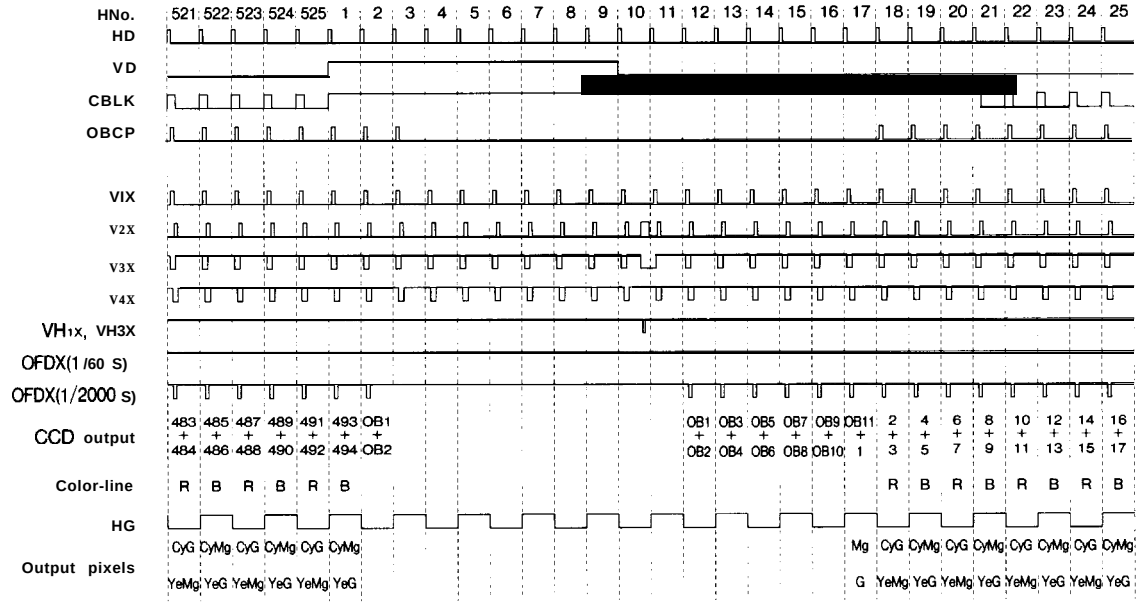
PAL : (1st, 3rd FIELD)

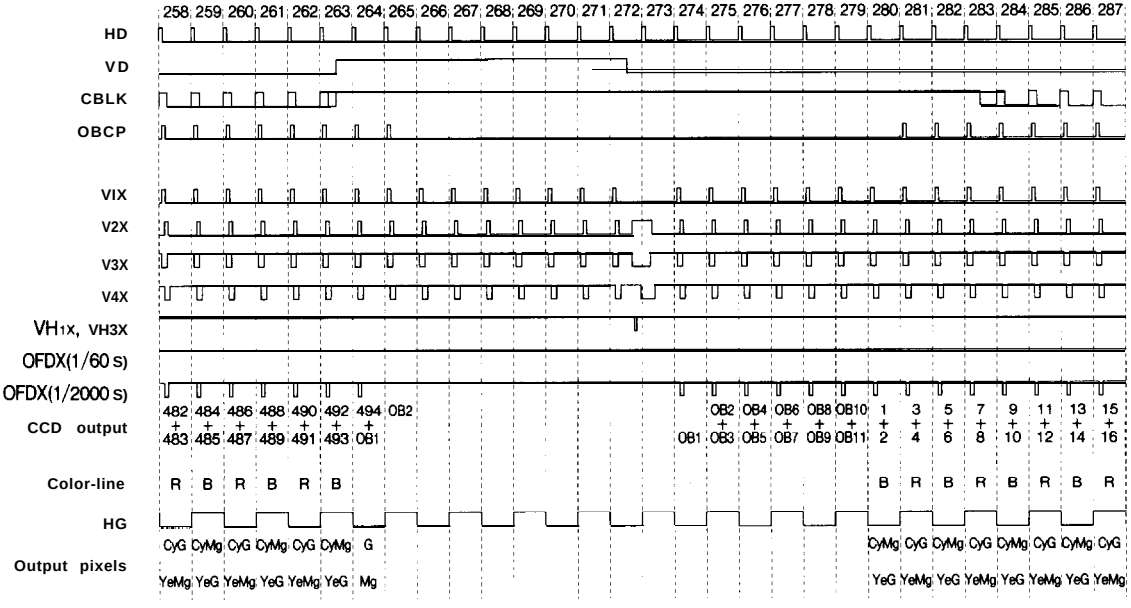


(2nd, 4th FIELD)

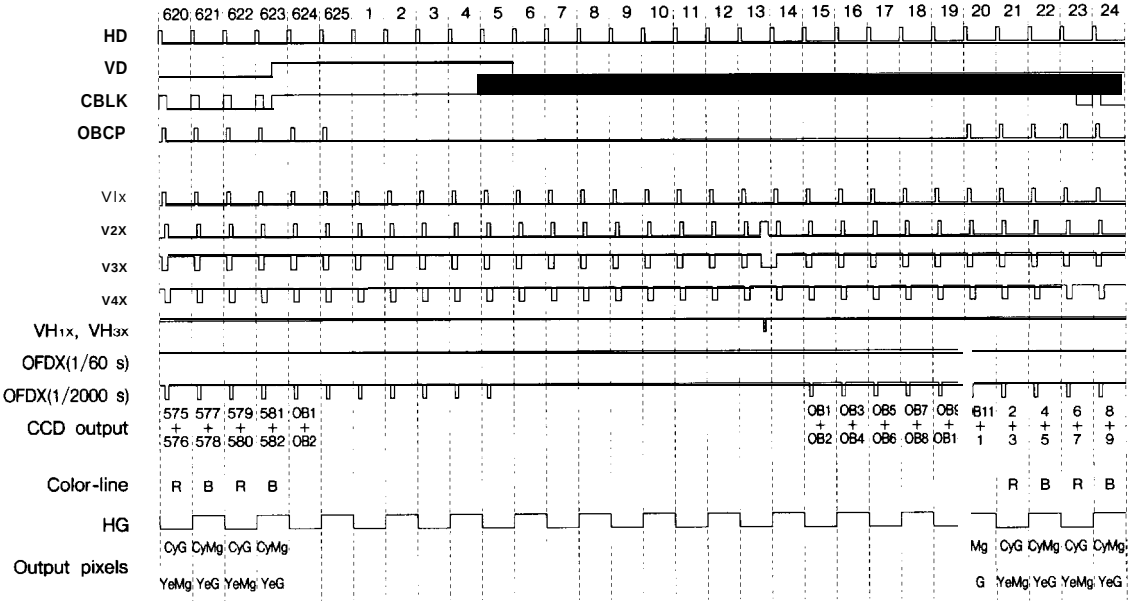


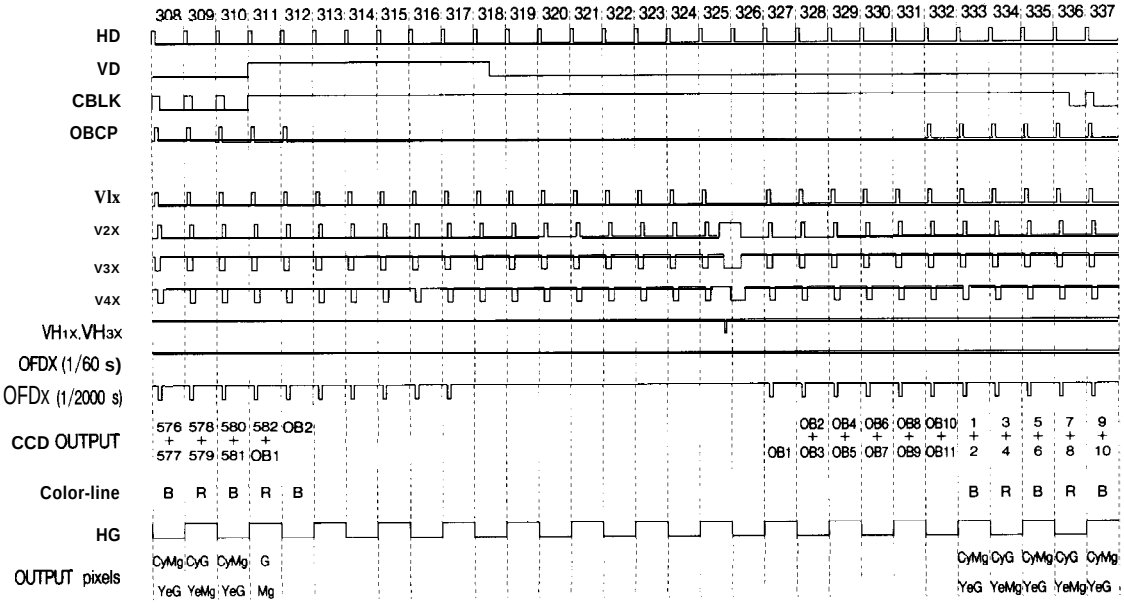
VERTICAL PULSE FOR DRIVING CCD < NTSC >





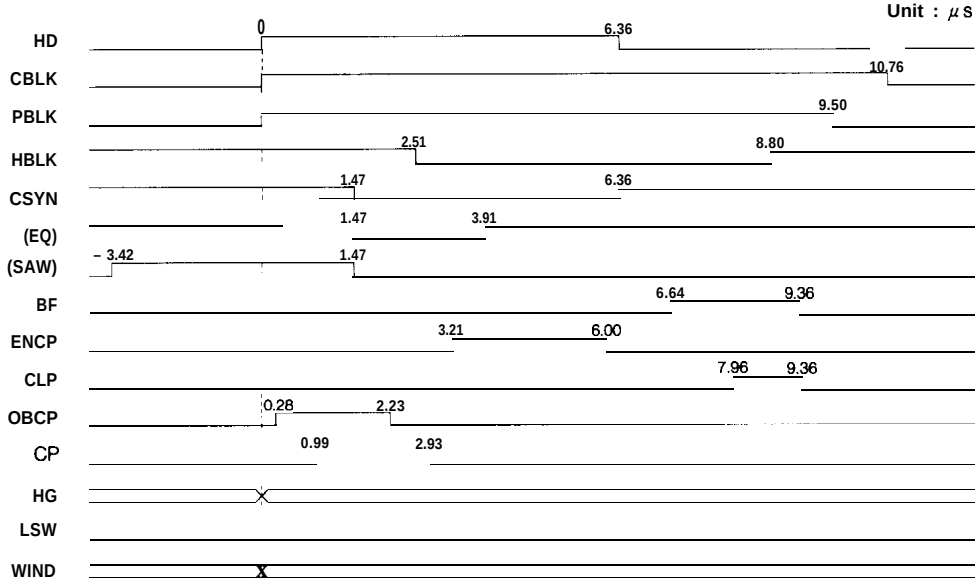
VERTICAL PULSE FOR DRIVING CCD < PAL >





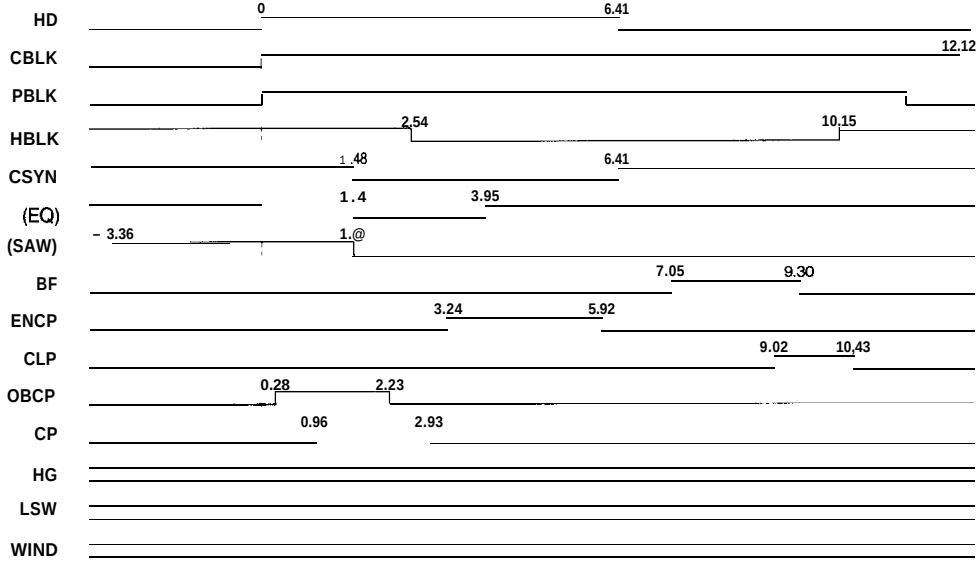
SYNCHRONIZING HORIZONTAL PULSE < NTSC >

Unit : μs

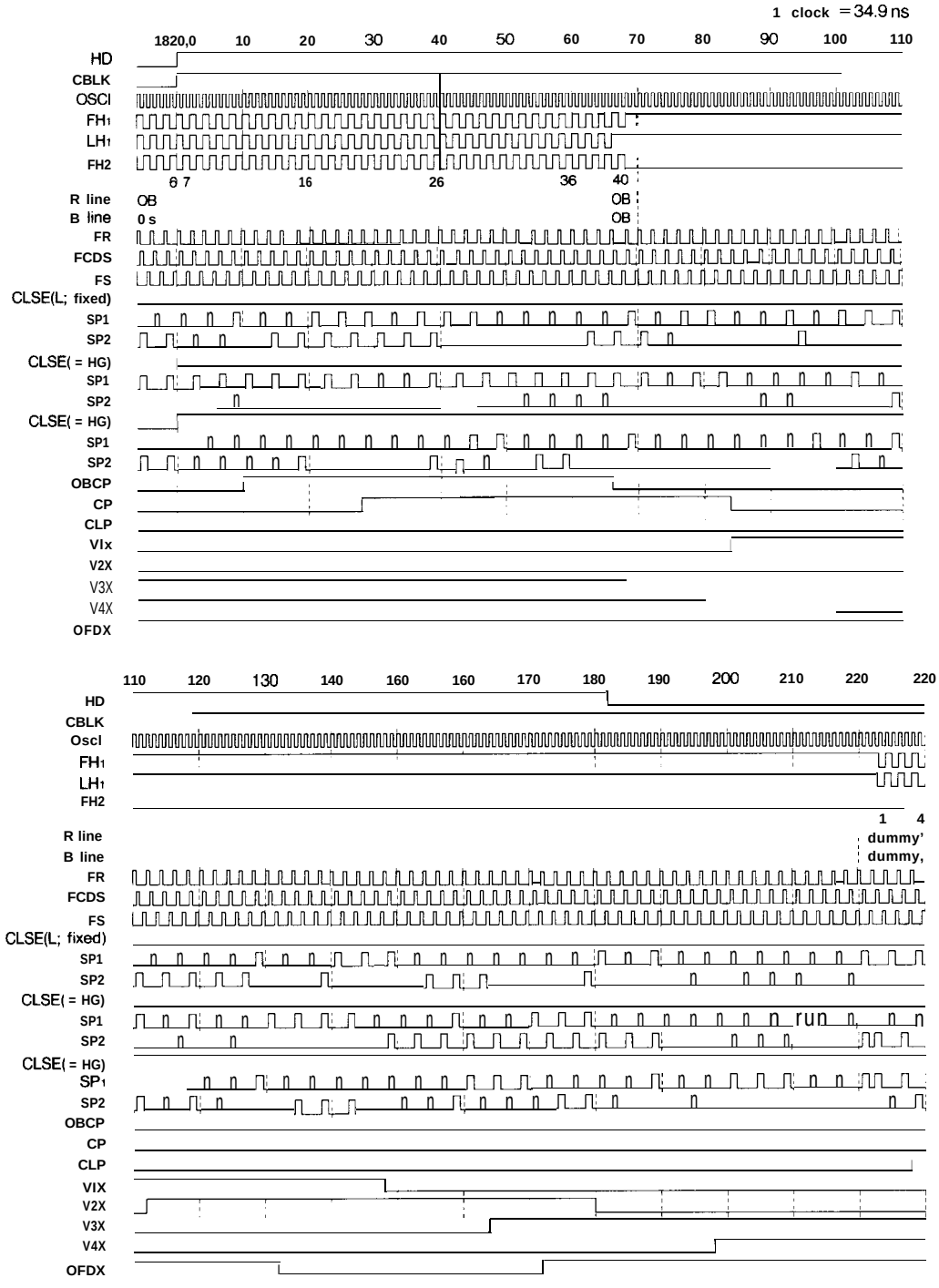


SYNCHRONIZING HORIZONTAL PULSE < PAL >

Unit : μs

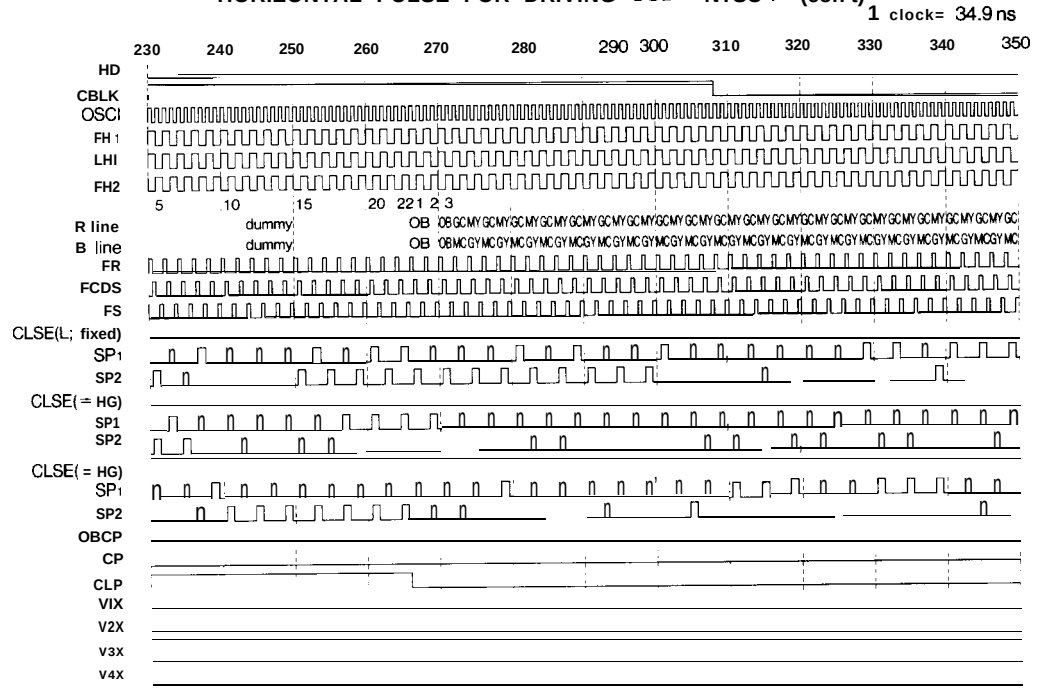


HORIZONTAL PULSE FOR DRIVING CCD < NTSC >



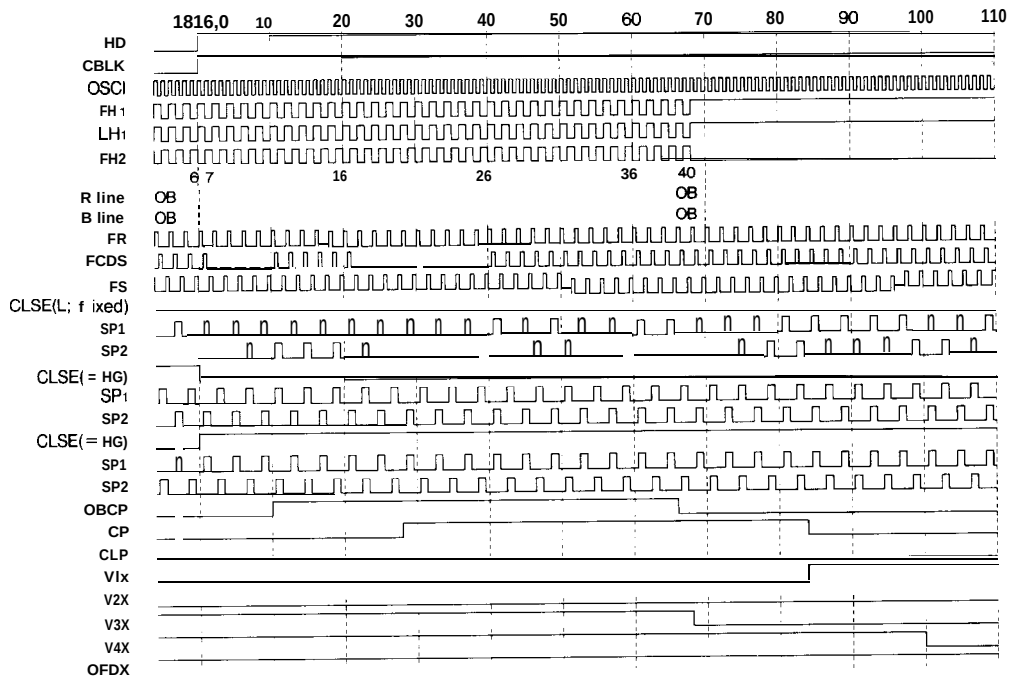
At SESL=L : When SESL=H, SP1 and SP2 is delayed about 35 ns.

HORIZONTAL PULSE FOR DRIVING CCD< NTSC > (con't)



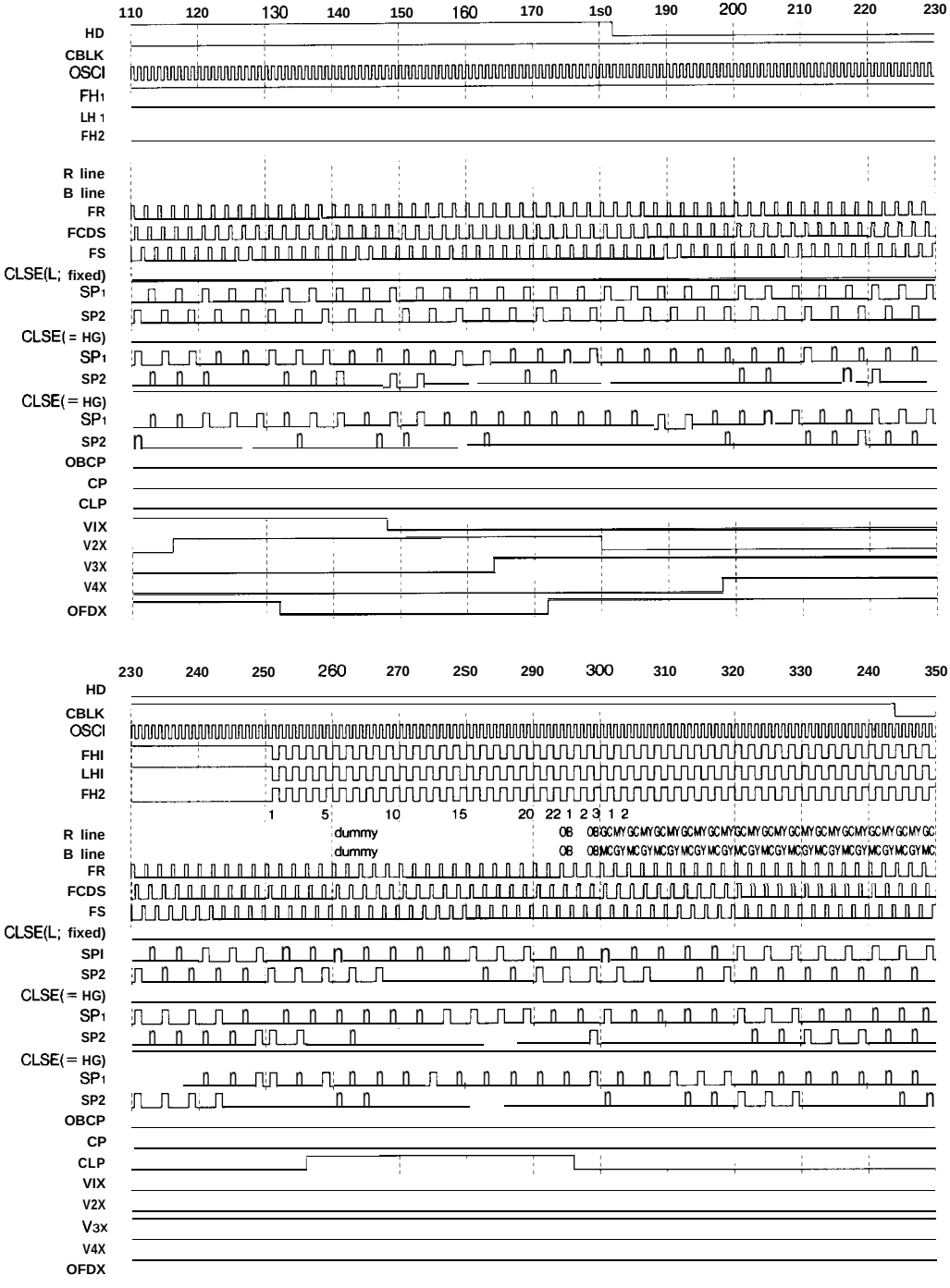
At SESL=L : When SESL=H, SPI and SP2 is delayed about 35 ns.

HORIZONTAL PULSE FOR DRIVING CCD< PAL >



At SESL=L : When SESL=H, SPI and SP2 is delayed about 35 na.

HORIZONTAL PULSE FOR DRIVING CCD < PAL > (cent'd) , clock = 35.2 ns

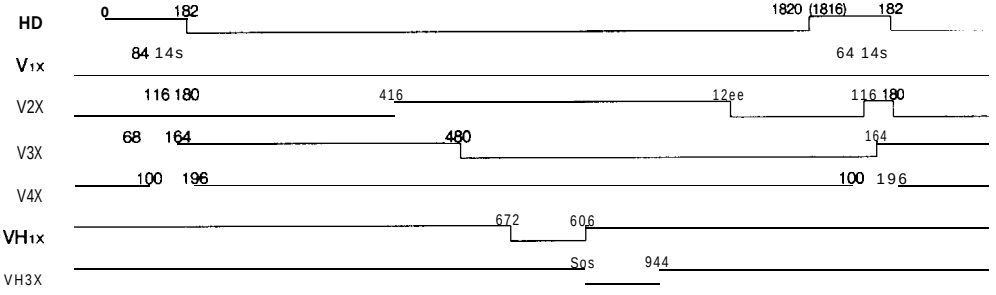


At SESL=L : When SESL=H, SP1 and SP2 is delayad about 35 na.

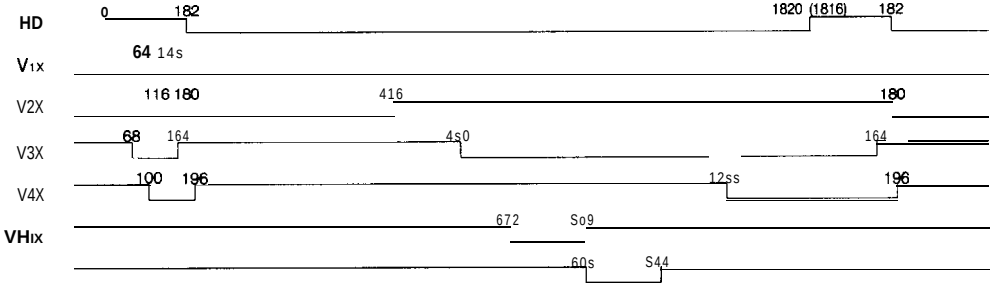
READ OUT PULSE

The number : OSCI clock pulse,
1 clock= 34,92 ns (35.24 ns), ( ) : PAL

(ODD (1st, 3rd) FIELD)

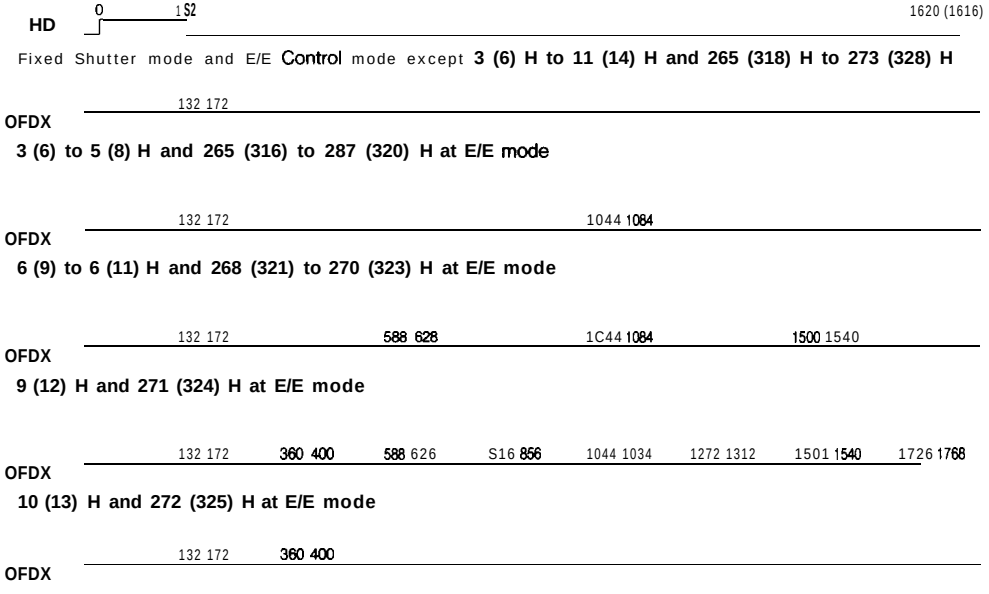


(EVEN (2nd, 4th) FIELD)

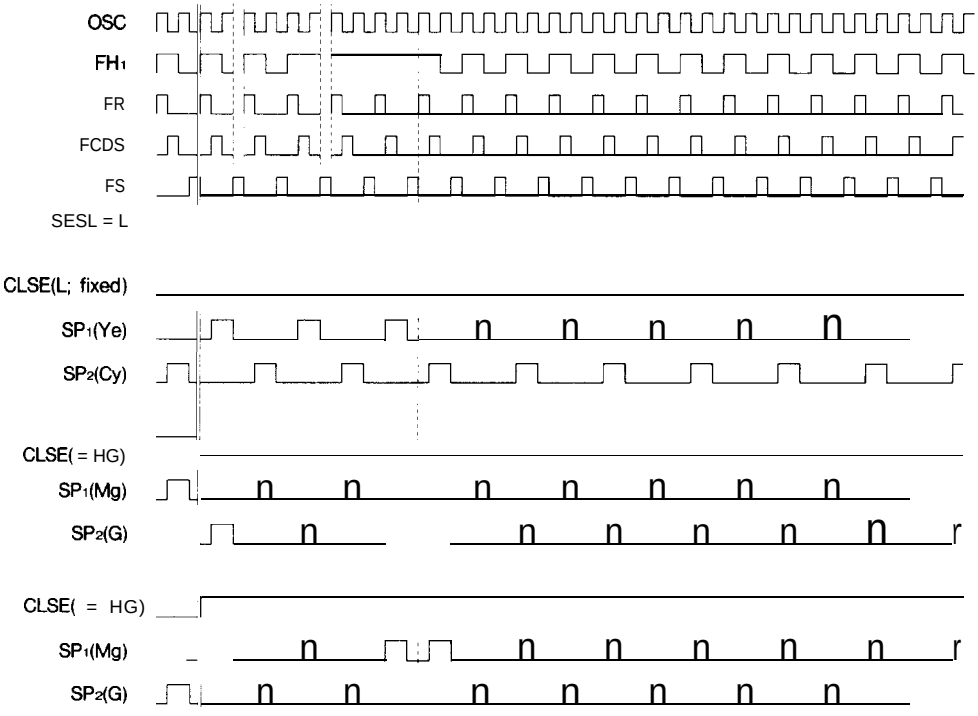


SHUTTER PULSE

The number : OSCI clock pulse,
1 clock= 34.92 ns (35.24 ns), ( ) : PAL



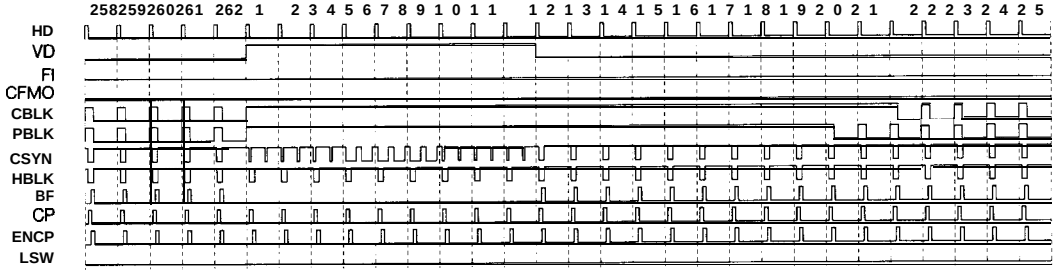
COLOR SEPARATE PULSE



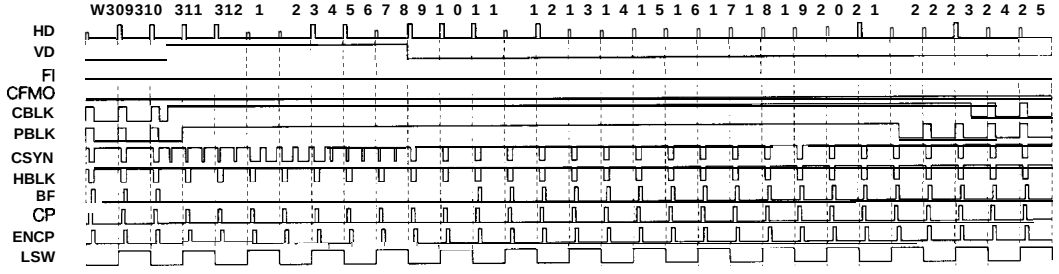
The SP2 pulse is delayed about 35 ns at SESL= H

NON-INTERLACE MOOE

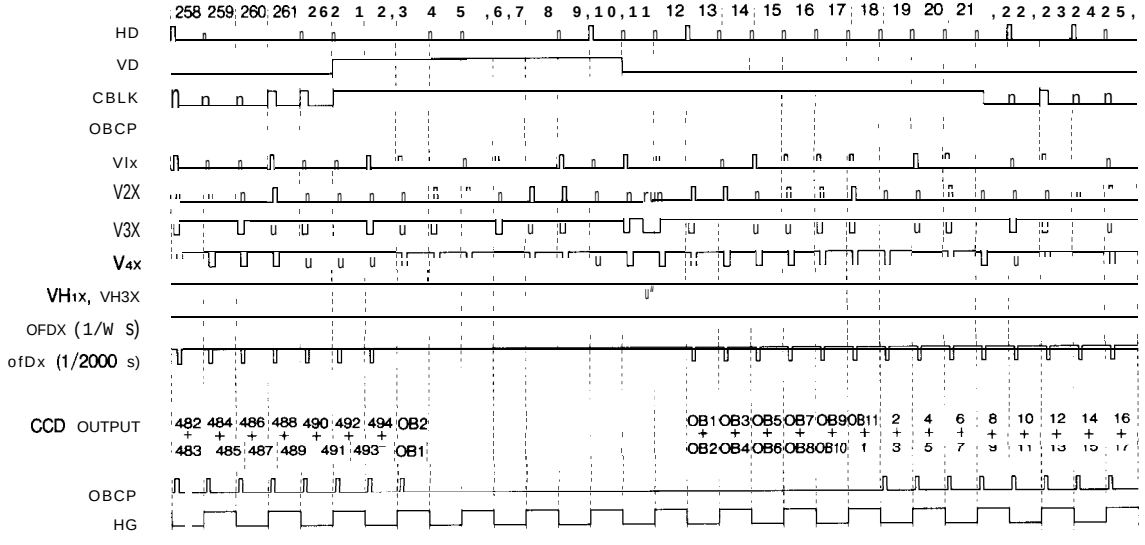
SYNCHRONIZING VERTICAL PULSE < NTSC >



SYNCHRONIZING VERTICAL PULSE < PAL >



VERTICAL PULSE FOR DRIVING CCD < NTSC >



NON-INTERLACE MODE (cent'd)

VERTICAL PULSE FOR DRIVING CCD < PAL >